the first conductive type to be a drain region. Then, a diffusion region 3 of a second conductive type referred to as a body region is formed from a surface of the semiconductor substrate by impurity implantation and high temperature thermal treatment at 1000°C or higher. Further, from the surface, a heavily doped impurity region 7 of the first conductive type to be a source region and a heavily doped body contact region 8 of the second conductive type for the purpose of fixing a potential of the body region by an ohmic contact are formed and are connected to a source electrode 7a and a body electrode 8a, respectively. Here, since a potential of the source region of the first conductive type and a potential of the body contact region of the second conductive type are usually the same, they are laid out so as to be in contact with each other in Fig. 2. The source electrode 7a and the body electrode 8a are connected with each other through a contact hole, not shown in the figure, for electrically contacting the two regions. Then, a trench 4 is formed by etching single crystalline silicon through the source region of the first conductive type. A gate insulating film 5 and polycrystalline silicon 6 containing a high concentration of impurity to be connected to a gate electrode 9a fill the silicon trench. The heavily doped region of the first conductive type on a rear side of the semiconductor substrate is connected to a drain electrode 1a.--

Please replace the paragraph beginning at page 5, line 9, with the following rewritten paragraph:

--According to another aspect of the present invention, the vertical MOS transistor is characterized in that a film other than a metal silicide is formed in the trench so as to be in contact with the polycrystalline silicon gate and surrounded by the gate insulating film and the polycrystalline silicon gate, the other film being formed of a silicon compound.--

Please replace the paragraph beginning at page 6, line 24, with the following rewritten paragraph:

--According to another aspect of the present invention, the method of manufacturing a vertical MOS transistor is characterized in that a film other than a metal silicide is formed on the polycrystalline silicon layer, such as a silicon oxide film.--

Please replace the paragraph beginning at page 11, line 17, with the following rewritten paragraph:

--Then, as a process specific to the present invention, first, the polycrystalline silicon 6 containing a high concentration of impurity is deposited at a thickness according to a width of the trench so as not to completely

fill the trench (Fig. 5). For example, when the width of the trench is 0.8 μm, the polycrystalline silicon is deposited to a thickness of 0.2 μm. The polycrystalline silicon containing a high concentration of impurity may be formed arbitrarily such as by implanting the impurity using thermal diffusion or ion implantation after polycrystalline silicon containing no impurity is deposited or by introducing the impurity while the polycrystalline silicon is being deposited.--

Please replace the paragraph beginning at page 14, line 10, with the following rewritten paragraph:

--First, since the gate has a laminated structure of the conventionally used polycrystalline silicon film and the metal silicide film, the gate resistance value can be lowered to 20% or less of that of the conventional art with only the polycrystalline silicon film. Especially, since the metal silicide reaches near the channel at a bottom portion of the trench, the inversion/depletion operation of the channel is fast, and turn-on characteristics and turn-off characteristics are improved. This allows a faster vertical MOS transistor, and operation at the level of MHz can be carried out effectively.--